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(54) Method and arrangement for calibrating an active filter

(57) The invention relates to a calibration method and a calibration arrangement for an active filter intended to be used especially in portable radio apparatus. The filter (100) according to the invention is an active RC filter and it is integrated except for one or more of its capacitances or one or more of its resistances. Advantageously the highest capacitance or the highest resistance is left unintegrated. when using an external capacitance, the principle of the calibration is as follows: The integrated resistances are corrected using a common coefficient such that the external capacitance together with the integrated resistances produces the correct time constants (1). Then the integrated capacitances are corrected using a common coefficient such that they together with the internal resistances that were corrected in the previous phase produce the correct time constants (2). If the filter comprises multiple circuit stages, the two-phase calibration process described above is repeated for each circuit stage.

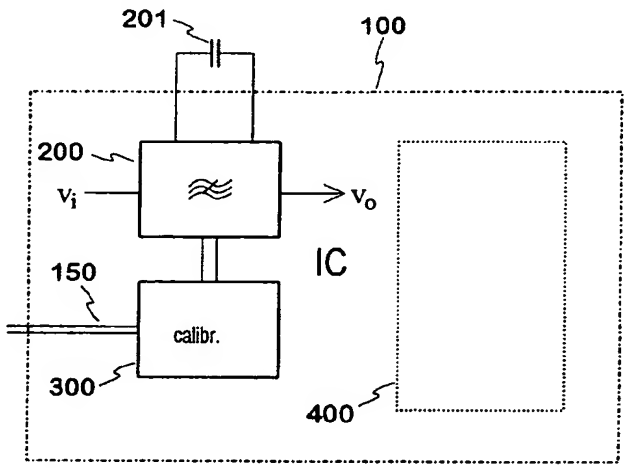

Fig. 1

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Description

[0001] The invention relates to a calibrating method defined in the preambles of claims 1 and 2 for an active filter intended to be used especially in portable radio apparatus. The invention also relates to a calibration arrangement for an active filter, defined in the preambles of claims 9 and 10.

[0002] Conventionally, low-frequency filters have been manufactured passive also. Their disadvantages include in particular the non-idealness caused by coils, the large size and relatively high production costs. Active filters realized using discrete components do not have the disadvantages caused by coils, but because of the number of components they, too, are space-consuming and have relatively high production costs.

[0003] An active filter can be realized in a small space by integrating it to a microcircuit. The problem with such filters is the large area required by the capacitances on the chip. Integration is possible if the capacitances are made very small and correspondingly the resistances very big. This means, however, that the signal level will drop and the noise level will increase and, therefore, this solution is usually unacceptable. Integration is possible also if small capacitances are used with very high virtual resistances based on the switched capacitor (SC) or switched current (SI) technology, for example. This eliminates high thermal noise levels, but the use of switches will result in the increase of noise level, increased current consumption and deterioration of the linearity of the filter. The latter will limit the dynamic range of the filter. If the apparatus in question is a radio device, the use of switches may also cause interference problems in the RF circuits of the apparatus. The filter may also be made such that the parts that are difficult to integrate are left outside the microcircuit. A disadvantage of such a construction is that calibration becomes more difficult; The filter requirements are usually so strict that, regardless of the construction, calibration is necessary because of the variation in component values. In the mixed construction mentioned above the deviations of the values of discrete and integrated components do not correlate, which means the calibration of filters in production may cause higher costs than totally discrete or totally integrated filters.

[0004] It is an object of the invention to eliminate above-mentioned disadvantages related to the prior art. The basic idea of the invention is as follows: The filter is an active RC filter and it is integrated except for one or more of its capacitances or one or more of its resistances. Advantageously the highest capacitance or highest resistance is left unintegrated. Each external capacitance is advantageously realized by a chip capacitor placed beside the integrated circuit. The principle of calibration, when using an external capacitance, is as follows: Integrated resistances are corrected by a common coefficient such that the external capacitance produces the correct time constants with them. Then the integrated capacitances are corrected by a common coefficient such that they produce the correct time constants with the internal resistances corrected in the previous phase. If the filter has multiple circuit stages, the two-phase calibration procedure described above is repeated for each circuit stage.

[0005] It is an advantage of the invention that the filter according to the invention can be made relatively small and it consumes a relatively small amount of energy. It is another advantage of the invention that the filter according to the invention is of good quality: It has a good signal-to-noise ratio, a large dynamic range, and it does not cause RF interference in its surroundings. It is a further advantage of the invention that the calibration of the filter can be adapted such that it is automatic and needs no external measuring instruments so that the calibration costs in the production are very low.

[0006] The method according to the invention for calibrating an active RC filter is characterized by what is expressed in the characterizing part of claim 1 or 2.

[0007] The active RC filter arrangement according to the invention is characterized by what is expressed in the characterizing part of claim 9 or 10. Preferred embodiments of the invention are presented in the dependent claims.

[0008] The invention will now be described in more detail with reference to the accompanying drawings wherein

- Fig. 1 shows a filter arrangement according to the invention,
- Fig. 2 illustrates the calibrating principle according to the invention,
- Fig. 3 shows an example of a filter circuit and calibrating circuit according to the invention,
- Fig. 4 illustrates in the form of flow diagram the operation of the calibrating circuit according to Fig. 3,
- Fig. 5 shows another example of a filter circuit and calibrating circuit according to the invention,
- Fig. 6 illustrates in the form of flow diagram the operation of the calibrating circuit according to Fig. 5, and
- Fig. 7 shows an example of a way of adjusting resistance and capacitance.

[0009] Fig. 1 shows a filter arrangement according to the invention comprising a microcircuit 100 which comprises a filter circuit 200, filter calibrating circuit 300 and possible other electronic circuits 400. Fig. 1 additionally shows a bus 150 for controlling the filter calibration and an external capacitor 201 of the filter, located outside the microcircuit. The external component in this example is a capacitor and there is just one of them.

[0010] The calibration of filters according to the invention is carried out by adjusting the time constants in phases. Fig. 2 shows component parts of a filter comprising two circuit stages 210 and 220. The detailed con-

struction of the filter is of no significance at this point. Circuit stage 210 comprises variable resistances R11 and R12, connected in series/longitudinally on the signal line, and variable capacitances C11 and C12, connected in parallel/transversely to the signal line. The circuit stage further comprises an external capacitance C1, connected to the rest of the filter via connector pins 101, 102 of the integrated circuit, and an amplifier stage A21. The second circuit stage 220 includes variable resistances R21 and R22, variable capacitances C21 and C22, an external capacitance C2 and an amplifier stage A22. Thus there are four phases in calibration of the filters. Let us assume that time constants R11·C1=T1, R12·C11=T2, R21·C2=T3 and R22·C21=T4 are critical for the filter's frequency response. In phase (1) the resistance R11 is adjusted, as well as the other resistances in circuit 210, until the time constant T1 is correct. In phase (2) the capacitance C11 is adjusted, as well as the other integrated capacitances in circuit 210, until the time constant T2 is correct. Correspondingly, in phase (3) the resistances in circuit 220 are adjusted until the time constant T3 is correct, and in phase (4) the integrated capacitances in circuit 220 are adjusted until the time constant T4 is correct. After that, the filter's frequency response is correct and the calibration of the filter is finished.

[0011] Fig. 3 shows a single-circuit-stage low-pass filter 200, 201, and its calibrating circuit 300. Both are examples of solutions according to the invention. The filter has an integrated part 200 and an external capacitor 201 (C1). By means of change-over switches kla and klb the latter can be made part of the filter or the calibrating circuit. The calibrating circuit 300 has an integrator 310, which comprises an amplifier Al, a comparator A2, logic unit 330 and a circuit 305 for generating reference voltages V_{ref1} and V_{ref2}. In the integrator 310 constant current is used to charge capacitance C1 or C_{ref}, depending on the phase of the calibration. The magnitude of the constant current depends on voltage V_{ref1} and resistance R_{ref}. In parallel with the capacitance charged there is a switch k3 by means of which the capacitance is discharged before a new charge cycle. Comparator A2 compares the integrator's output voltage v_1 with voltage V_{ref2} which is greater than V_{ref1}. If during the integration cycle voltage v_1 reaches voltage V_{ref2}, the comparator's output signal A is set to "1", otherwise it remains at "0". Comparator A2 is connected to the logic unit 330. From outside the microcircuit 100 a control signal START is brought to the logic unit to start the calibration process. The logic unit 330 controls the flow of the calibration on the basis of the state of the comparator's output signal A by setting the switches k1, k2 and k3 as well as the integrated resistance values by setting a control word S_r and the integrated capacitance values by setting a control word S_c.

[0012] Because of the manufacturing process the resistance values in the microcircuit deviate from their nominal values to the same direction and proportionally to the same extent. Similarly, the capacitance values deviate from their nominal values proportionally to the same extent. Because of this, the calibration may use the integrated reference resistance R_{ref} and capacitance C_{ref} instead of the component parts in the filter so that there will be no need to work with the integrated filter construction in order to adjust its component values. The resistances R1 and R2 in the filter construction and R_{ref} in the calibrating circuit are adjustable. The adjustment is carried out using a common control word S_r so that their values always change in proportion. Correspondingly, the capacitances C11 and C12 in the filter construction and C_{ref} in the calibrating circuit are adjustable by a common control word S_c.

[0013] Fig. 4 shows a flow diagram of the calibration process of the circuit in Fig. 3. After the start, in step 41 the external capacitance C1 is connected to be the capacitance of the integrator in the calibrating circuit. In step 42, the logic unit sends the value S_{rmax} representing the maximum resistances to the register controlling the resistance values. In step 43, switch k3 in parallel with the integrator's capacitance is closed, thereby discharging the possible charge of the capacitance and setting the integrator's output voltage v_1 to V_{ref1}. In step 44, the values of the internal resistances in the microcircuit are decremented by one step. This is of no significance during the first cycle of the process. Next, in step 45, switch k3 is opened, starting the charging of capacitance C1. Time is counted in step 46. After a predetermined time T1 the state of the output signal A of the comparator A2 is checked in step 47. If the output voltage v_1 of the integrator has not yet reached V_{ref2}, signal A is in state "0" and the voltage integration cycle is repeated using a resistance R_{ref} value one step smaller than before (steps 43 to 47). Time constant R_{ref}·C1 will then be a little smaller, making the voltage v_1 to increase a little faster than in the previous cycle. The cycle will be repeated until the voltage v_1 reaches V_{ref2} in time T1, indicated by state "1" of signal A. Parameter T1 is chosen such that time constant R1·C1 will then conform to the desired transfer function. The microcircuit's internal resistance values, R2 included, will not be changed after this.

[0014] Steps 48 to 54 in Fig. 4 represent the second phase of the calibration process. Certain values have to be set for time constants R2·C11 and R2·C12 in order to fulfill the desired transfer function of the exemplary filter. First, in step 48, external capacitance C1 is connected to its place in the filter and internal capacitance C_{ref} is connected to the integrator. The ratio of capacitance C_{ref} to capacitance C11 is known. Similarly, the ratio of resistances R_{ref} and R2 is known. Thus it is possible to determine the time T2 in which the integrator's output voltage should reach voltage V_{ref2} for time constant R2·C11 to be correct. The second phase of the calibration goes on in a similar manner as the first phase. Only, now the internal capacitances are first set to their maximum values, step 49, and then gradually

decreased until it is detected that signal A is in state "1", steps 50 to 54. Time constant R2·C11 is then correct. Time constant R2·C12 is also correct, because the ratio C12/C11 was correct from the beginning and it is not changed during the calibration. The end result of the calibration is that individual component values are not known but all critical time constants and resistance ratios are substantially correct.

[0015] Fig. 5 shows another calibrating arrangement according to the invention. In this example the filter 200, 201, 202 to be calibrated is a third-order low-pass filter comprising a first circuit stage 210, differential amplifier A2 and a second circuit stage 220. The first circuit stage 210 is a differential amplifier realized by transistors Q1 and Q2. It is integrated except for an external capacitor 201 (C1) which determines the cut-off frequency. Said capacitor can be connected by change-over switches kla, klb either to the calibrating circuit or to the filter. Calibration is directed to collector resistors R11, R12 in transistors Q1, Q2. The second circuit stage 220 is a second-order biquad-type filter realized by amplifier A3, as the filter in Fig. 3. It is integrated except for an external capacitor 202 (C2). Said capacitor can be connected by change-over switches k2a, k2b either to the calibrating circuit or to the filter. Calibration is directed to resistors R21, R22 and capacitors C21, C22. The calibrating arrangement in Fig. 5 comprises an integrated calibrating circuit 300 and an external calibrating system 500. The calibrating circuit 300 comprises a differential amplifier A1, reference resistor R_{ref}, reference capacitor C_{ref}, register unit 350 and switches k3, k4 and k5. The register unit 350 comprises registers k, S_{r1}, S_{r2} and S_c. S_{r1}, S_{r2} and S_c also represent the contents of the respective registers. The external system 500 comprises a control unit 510, digital-to-analog converter 520, analog-to-digital converter 530 and a bus 540. The control unit 510 comprises a memory 511 in which a calibrating program PR is stored. The output voltage V_g of the digital-to-analog converter is taken to the differential amplifier A1 in the calibrating circuit 300. The calibration measurement voltage V_m is brought from the calibrating circuit 300 to the analog-to-digital converter 530. Converter 520 is controlled and converter 530 is read through bus 540. The bus 540 also extends to the register unit 350 in the calibrating circuit 300.

[0016] If the filter to be calibrated belongs to a digital mobile communications device, the digital-to-analog converter 520 is preferably a converter in the modulator of the mobile communications device. Similarly, the analog-to-digital converter 530 is preferably a converter in the demodulator of the mobile communications device. The control unit 510 and its memory may in that case belong to the mobile communications device or they may reside in a separate apparatus.

[0017] Adjustment of filter time constants in the example of Fig. 5 is based on checking the frequency responses of the first-order RC circuits from signal amplitudes. To that end, the external system 500 generates a sinusoidal voltage V_g such that the control unit 510 feeds to the digital-to-analog converter 520 a number sequence from the memory 511 which corresponds to samples taken from the sine wave. The converter 520 is controlled at such a rate that the frequency of the sine wave V_g generated is in the same order of magnitude as the cut-off frequency of the low-pass filter to be calibrated. The voltage V_g is taken via a differential amplifier AI to the input of a first-order RC low-pas filter. The low-pass filter comprises, series connected, resistor R_{ref} and one of capacitors C1, C2 and C_{ref}. Selection is made with switches kl, k2, k3 and k4. The position of the switches depends on the number sent by the control unit 510 to register k in the register unit 350. The output voltage V_m of the low-pass filter is taken from between resistor R_{ref} and capacitor C_n (n = 1, 2, ref). The voltage V_m is led to the analog-to-digital converter 530. The control unit 510 reads the converter 530 and produces on the basis of the numbers received a reference number that corresponds to the amplitude of voltage V_m.

[0018] The calibrating circuit 300 includes a switch k5 connected in parallel with resistor R_{ref}. When the switch is closed, voltage V_m becomes the output voltage of the differential amplifier A1. Let this unattenuated voltage be V_0. When switch k5 is open, voltage V_m is smaller than voltage V_0 because of the attenuation caused by the filter R_{ref}, C_n. Let this attenuated voltage be V_n. The control unit calculates on the basis of the values of voltages V_0 and V_n the time constant $R_{ref}·C_n = T_n$ of the filter R_{ref}, C_n being measured. Naturally the frequency value, which is in the control unit's memory, is also needed in the calculation. From the time constants T_n the control unit further calculates coefficients for the integrated resistors and capacitors such that all time constants of the filter calibrated are substantially correct. The control unit 510 sends said coefficients to the register unit 350. Number S_{r1} determines the resistance values R11 and R12 in circuit stage 210, number S_{r2} determines the resistance values R21 and R22 in circuit stage 220, and number S_c determines the capacitance values C21 and C22 in circuit stage 220.

[0019] The calibrating process for the structure in Fig. 5 is in accordance with Fig. 6, for example. Step 61 comprises preliminary actions such as activating the functional units and starting the generation of the sine wave used in the measurements. In step 62 variable n, which indicates the phase of the calibration, is set to state 0. This causes switch k5 to close so that the measurement signal Vg will bypass the filters used in the measurement. In addition, step 62 comprises a certain delay $\Delta t1$ so that voltage V_m will have time to settle before the analog-to-digital converter 530 is read. That reading takes place in step 63. As a result of the read, the calibration control program PR generates a voltage value V_0 in which there is no attenuation caused by the filter measured. In step 64 the value of variable n is increased by one, which represents a transition to the next calibration phase. In phases 1, 2 and 3 the process sets the regis-

ters in the register unit 350 as needed (step 66), waits for a certain period of time $\Delta t2$ (step 67), reads the converter 530 (step 68) and generates a value V_n for the voltage measured. When n is one, change-over switches kla, klb and k3 are set to state 1 and switches k4 and k5 are set to "open" so that external capacitor C1 of the microcircuit 100 is connected in series with resistor R_{ref} and the other end of the capacitor is connected to ground. On the basis of measurement result V_1 the program PR calculates a calibration coefficient for resistors R11, R12 in circuit stage 210. When variable n is two, change-over switches k2a and k2b are set to state 1 and change-over switch k3 to state 2 so that external capacitor C2 of the microcircuit 100 is connected in series with resistor R_{ref} and the other end of the capacitor is connected to ground. On the basis of measurement result V_2 the program PR calculates a calibration coefficient for resistors R21, R22 in circuit stage 220. At this phase the value of resistance R_{ref} has to be changed according to the coefficient mentioned above. When variable n is three, change-over switches k1a, k1b, k2a and k2b are set to state 2 and switch k4 to state "closed" so that an integrated reference capacitor C_{ref} is connected in series with resistor R_{ref} such that the other end of said capacitor is fixed to ground. On the basis of measurement result V_3 the program PR calculates a calibration coefficient for capacitors C21, C22 in circuit stage 220. When variable n is four, the process in this example enters in accordance with step 65 the final calibration phase 69 in which the generation of the measurement signal V_g is ceased, among other things. The calibration coefficients loaded into registers Sr1, Sr2 and Sc remain in the registers.

[0020] The examples depicted in Figs. 5 and 6 have one filter to be calibrated. If, for example, the apparatus has got quadrature branches for the baseband signal, there are two similar filters to be calibrated which are preferably integrated on one circuit. There will then be more calibration phases, of course. If, for example, the filters are as in Fig. 5, the calibration of the resistances of both circuit stages in both filters need phases of their own. However, one measurement will suffice to set the capacitances of the latter circuit stages.

[0021] Fig. 7 shows an example of how the internal resistances and capacitances in the microcircuit can be adjusted. Fig. 7a shows a variable resistance. It comprises six resistances R_a, R_b, R_c, R_d, R_e and R_f in series which, except for resistance R_a, can be short-circuited. Resistance R_b can be short-circuited by switch k_b which is controlled by a digital signal b0. Correspondingly, resistance R_c can be short-circuited by switch k_c controlled by a digital signal bl, etc. Thus the overall resistance R is derived as follows:

$$R = R_a + b0 \cdot R_b + b1 \cdot R_c + b2 \cdot R_d + b3 \cdot R_e + b4 \cdot R_f.$$

[0022] State "0" of bits b0 to b4 corresponds to open switch and state "1" corresponds to closed switch. Then the byte b0 b1 b2 b3 b4 corresponds in Figs. 3 to 6 to the resistance control signal R_r. When all bits are "ones", the resistance is at the highest ($R_{max} = R_a + R_b + R_c + R_d + R_e + R_f$), and when all bits are zeros, the resistance is at the lowest ($R_{min} = R_a$). Let us assume that the overall tolerance of the product of the external capacitance and the integrated resistance is about ±25%. Then the circuit is manufactured e.g. in such a manner that $R_b = 0.32R_a$, $R_c = 0.16R_a$, $R_d = 0.08R_a$, $R_e = 0.04R_a$ and $R_f = 0.02R_a$. Now the control byte b0...b4 can be used to choose the resistance from the range $R_a...1.6R_a$ with a resolution of $0.02R_a$. The value $1.3R_a$ corresponds to the nominal value of the resistance in question. Naturally the resolution of the adjustment can be improved by increasing the number of resistances, switches and control bits.

[0023] Fig. 7b shows an example of a variable capacitance. The arrangement is similar to the one above. For the total capacitance we get

$$C = C_a + b0 \cdot C_b + b1 \cdot C_c + b2 \cdot C_d + b3 \cdot C_e + b4 \cdot C_f.$$

[0024] Byte b0 b1 b2 b3 b4 now corresponds to the capacitance control signal S_c in Figs. 3 to 6. The partial capacitances are chosen such that the adjustment range of the total capacitance covers the tolerance for the product of the integrated resistance and capacitance added to the tolerance for the external capacitance.

[0025] Above it was described examples of filter calibration according to the invention. The invention is not limited to the arrangements described above. The filter may as well be any analog active filter the operation of which is not based on clock signals such as the clock signals of SC filters. It is possible to have various implementations for the measuring circuits that are used in the calibration circuit of the filter for measuring the charging time of the capacitor or the attenuation of the sine voltage. It is possible to control the time constants of the filter directly by adding switches without using integrated reference components. Calibration can also be controlled using a program run in a separate processor circuit instead of the processor circuit belonging to the measured equipment. The structures of the variable resistances and capacitances may differ from those described. The inventional idea can be applied in various cases defined by the claims set forth below.

Claims

1. A method for calibrating an active filter (200, 201) wherein at least one resistance (R11) and one capacitance (C11) of the component parts of said filter are provided in an integrated circuit (100), and at least one capacitive component (201; C1) is placed outside the integrated circuit (100), **characterized**

in that

- said at least one integrated resistance is adjusted until it produces together with the external capacitance (201) a predetermined time constant, and
- after that, said at least one integrated capacitance is adjusted until it produces together with said integrated resistance(s) a predetermined time constant.

2. A method for calibrating an active filter wherein component parts of said filter are used for providing at least one capacitance and one resistance in an integrated circuit, and at least one resistive component is placed outside said integrated circuit, **characterized** in that

- said at least one integrated capacitance is adjusted until it produces together with said external resistance a predetermined time constant, and
- after that, said at least one integrated resistance is adjusted until it produces together with said at least one integrated capacitance a predetermined time constant.

3. The method of claims 1 and 2, **characterized** in that

- the variable resistances are first set to their boundary values (42) and then gradually changed (44) until the observed time constants are correct, and
- the variable capacitances are first set to their boundary values (49) and then gradually changed (51) until the observed time constants are correct.

4. The method of claims 1 and 2, **characterized** in that

- it is determined the attenuation at a given frequency of the first-order filter corresponding to the time constant being adjusted,
- it is calculated on the basis of said attenuation a correction coefficient for the component value on which said time constant depends, and
- it is set for said component value the value that corresponds to said correction coefficient.

5. The method of claim 1 or 2 wherein a filter is comprised of at least two successive circuit stages (210, 220), **characterized** in that said two-phase adjustment of component values is carried out separately in each circuit stage.

6. The method of any one of claims 1 to 5 wherein a reference resistance (R_{ref}) and reference capacitance (C_{ref}) are produced in said integrated circuit (100), **characterized** in that said reference elements are used in calibration measurements instead of the integrated filter elements being adjusted.

7. The method of any one of claims 1 to 6, **characterized** in that during the calibration

- said reference resistance and the filter's integrated resistances being adjusted at that particular time are adjusted by a common control signal (S_r),and
- said reference capacitance and the filter's integrated capacitances being adjusted at that particular time are adjusted by a common control signal (S_c).

8. The method of any one of claims 1 to 3 or 5 to 7, **characterized** in that the detection of the correctness of said time constants (47, 54) and said adjustment of the filter's component values are carried out in the same integrated circuit (100).

9. The method of claims 1 to 8, **characterized** in that the integrated resistances (R11, R12, ...) and capacitances (C11, C12, ...) are adjusted by connecting the component parts in question in series and/or in parallel.

10. An arrangement for calibrating an active filter (200, 201) that comprises at least one integrated resistance (R11), at least one integrated capacitance (C11) and at least one external capacitive component (C1), **characterized** in that it comprises

- means for adjusting said at least one integrated resistance in such a manner that it produces together with said external capacitance a predetermined time constant, and
- means for adjusting said at least one integrated capacitance in such a manner that it produces together with said at least one integrated resistance a predetermined time constant.

11. An arrangement for calibrating an active filter that comprises at least one integrated capacitance, at least one integrated resistance and at least one external resistive component, **characterized** in that it comprises

- means for adjusting said at least one integrated capacitance in such a manner that it produces together with said external resistance a predetermined time constant, and
- means for adjusting said at least one integrated resistance in such a manner that it produces together with said at least one integrated capacitance a predetermined time constant.

12. The arrangement of claim 10 or 11, **characterized** in that said means for adjusting the integrated resistances and capacitances comprises a RC time constant measuring circuit.

13. The arrangement of claim 12, **characterized** in that said time constant measuring circuit comprises a constant voltage source (305), an analog integrator (310) and an analog comparator.

14. The arrangement of claim 10 or 11, **characterized** in that said means for adjusting the integrated resistances and capacitances comprises means for determining the attenuation of a RC circuit at a given frequency.

15. The arrangement of claim 14, **characterized** in that the means for determining said attenuation comprises a set of digital numbers corresponding to a sine wave, digital-to-analog converter (520), analog-to-digital converter (530) and a program (PR) for controlling said converters and calculating the magnitude of an alternating voltage (V_m) on the basis of samples.

16. The arrangement of claim 15, **characterized** in that said converters (520, 530) are primarily arranged so as to process a modulating and detected signal in a radio apparatus to which the filter to be calibrated belongs.

17. The arrangement of any one of claims 10 to 14, **characterized** in that the control means for adjusting the integrated resistances and capacitances is a logic unit (330) integrated into the same circuit (100) with the filter circuit.

18. The arrangement of any one of claims 10 to 15, **characterized** in that the control means for adjusting the integrated resistances and capacitances is a processor equipped with an appropriate program.

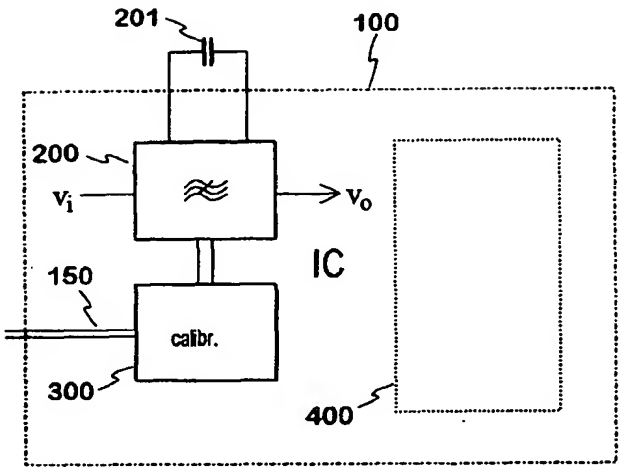


Fig. 1

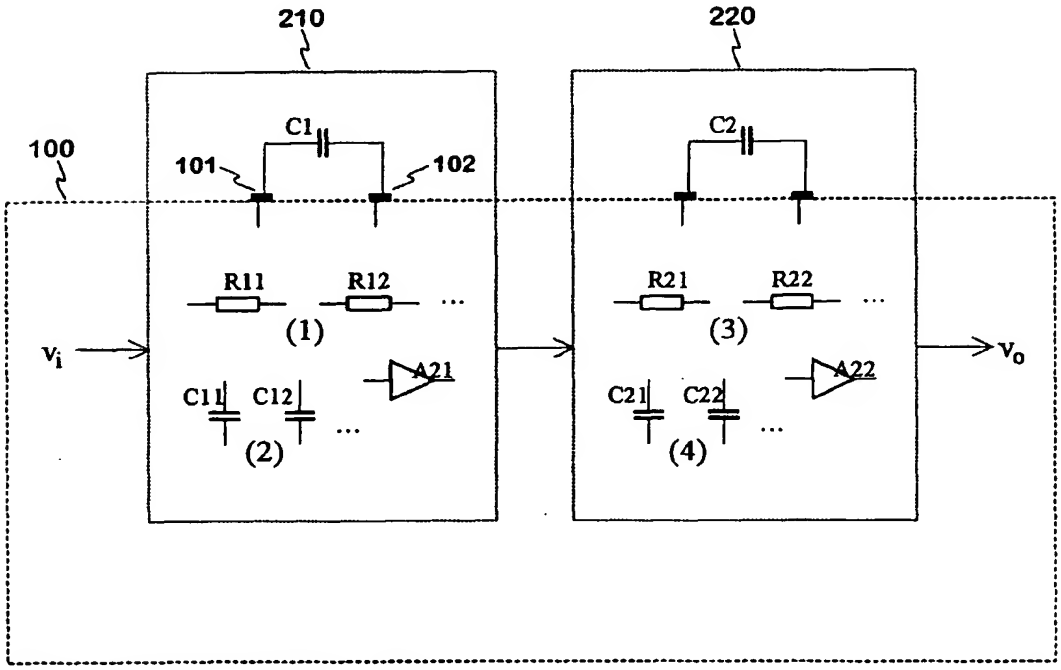
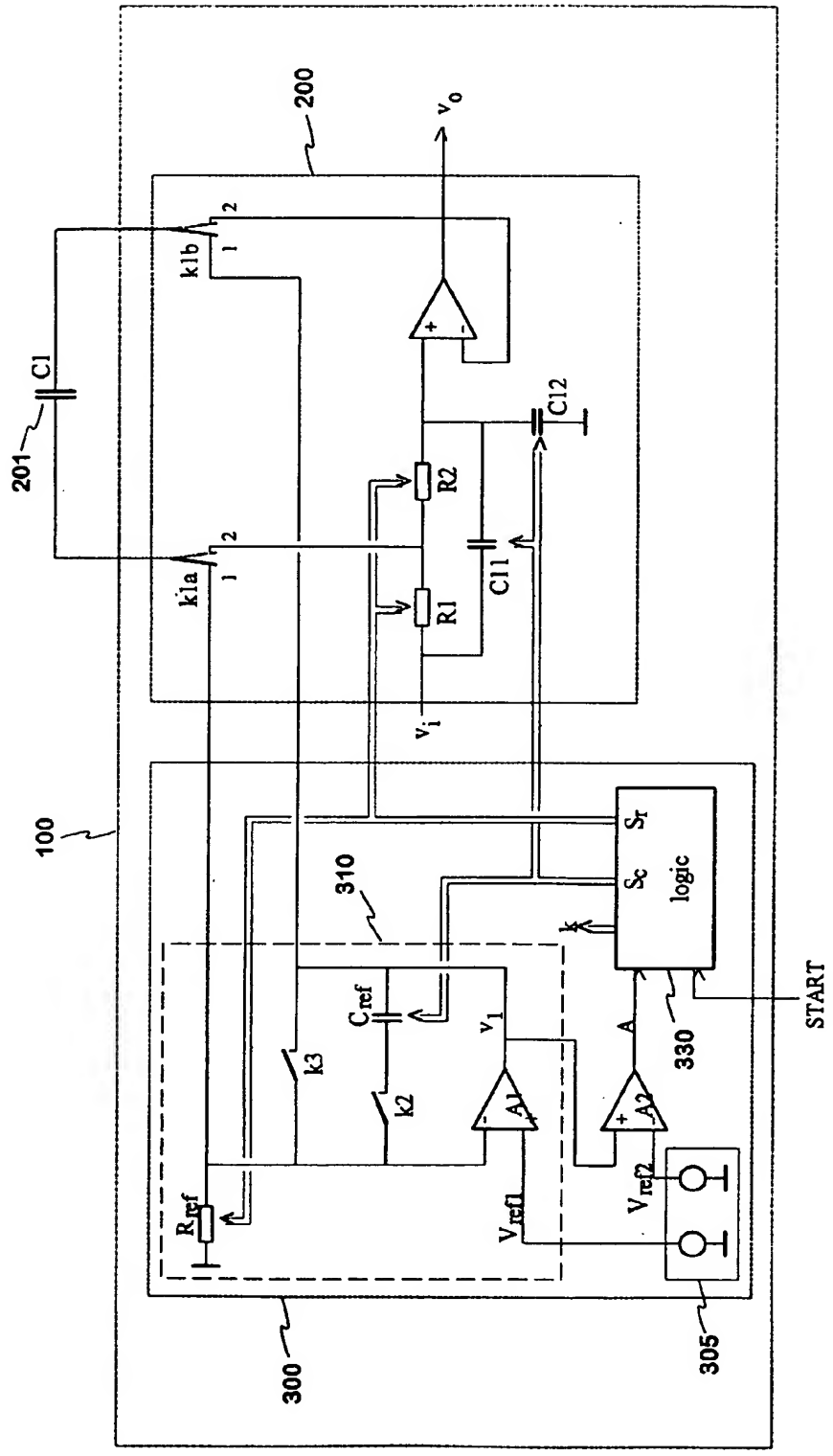


Fig. 2

calibration phases (1), (2), (3) and (4)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C1
201
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R2
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R1
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logic
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V_{ref2}
300
305

Fig. 3

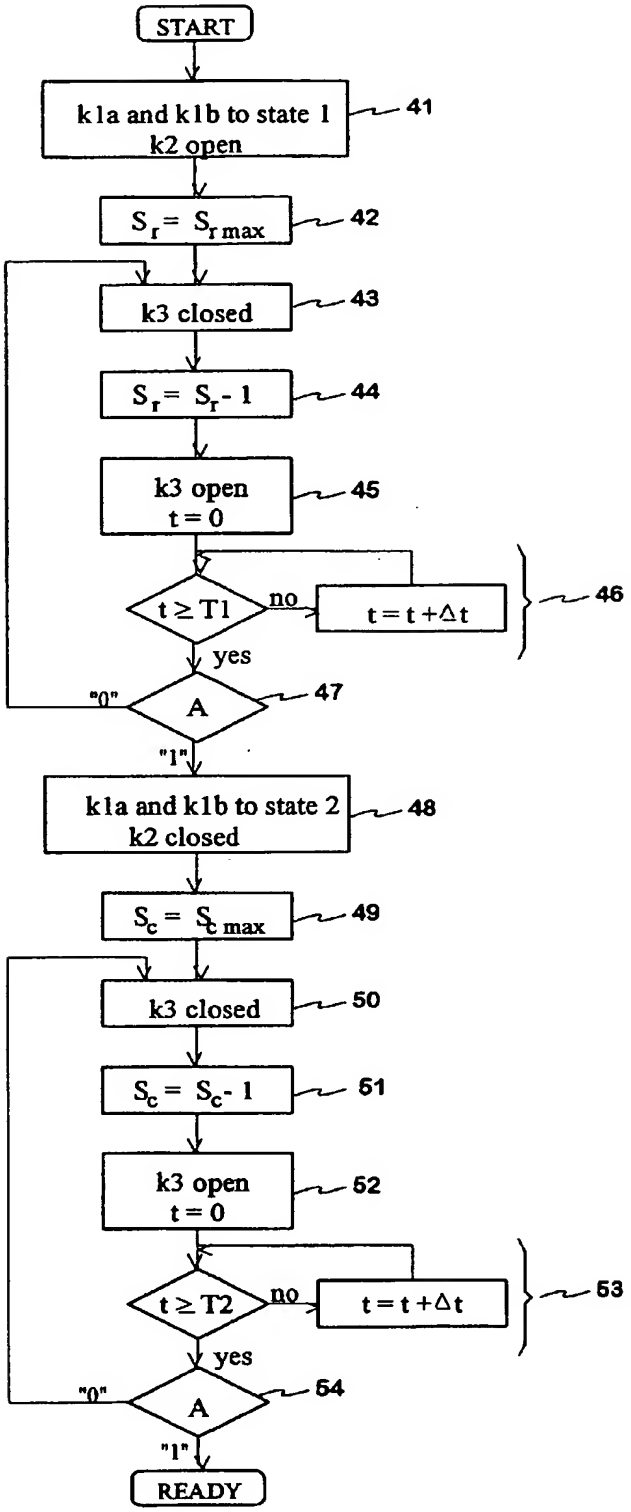

START
k1a and k1b to state 1
k2 open
41
$S_r = S_{r\,max}$
42
k3 closed
43
$S_r = S_r - 1$
44
k3 open
t = 0
45
t ≥ T1
no
t = t + Δt
46
yes
"0"
A
47
"1"
k1a and k1b to state 2
k2 closed
48
$S_c = S_{c\,max}$
49
k3 closed
50
$S_c = S_c - 1$
51
k3 open
t = 0
52
t ≥ T2
no
t = t + Δt
53
yes
"0"
A
54
"1"
READY

Fig. 4

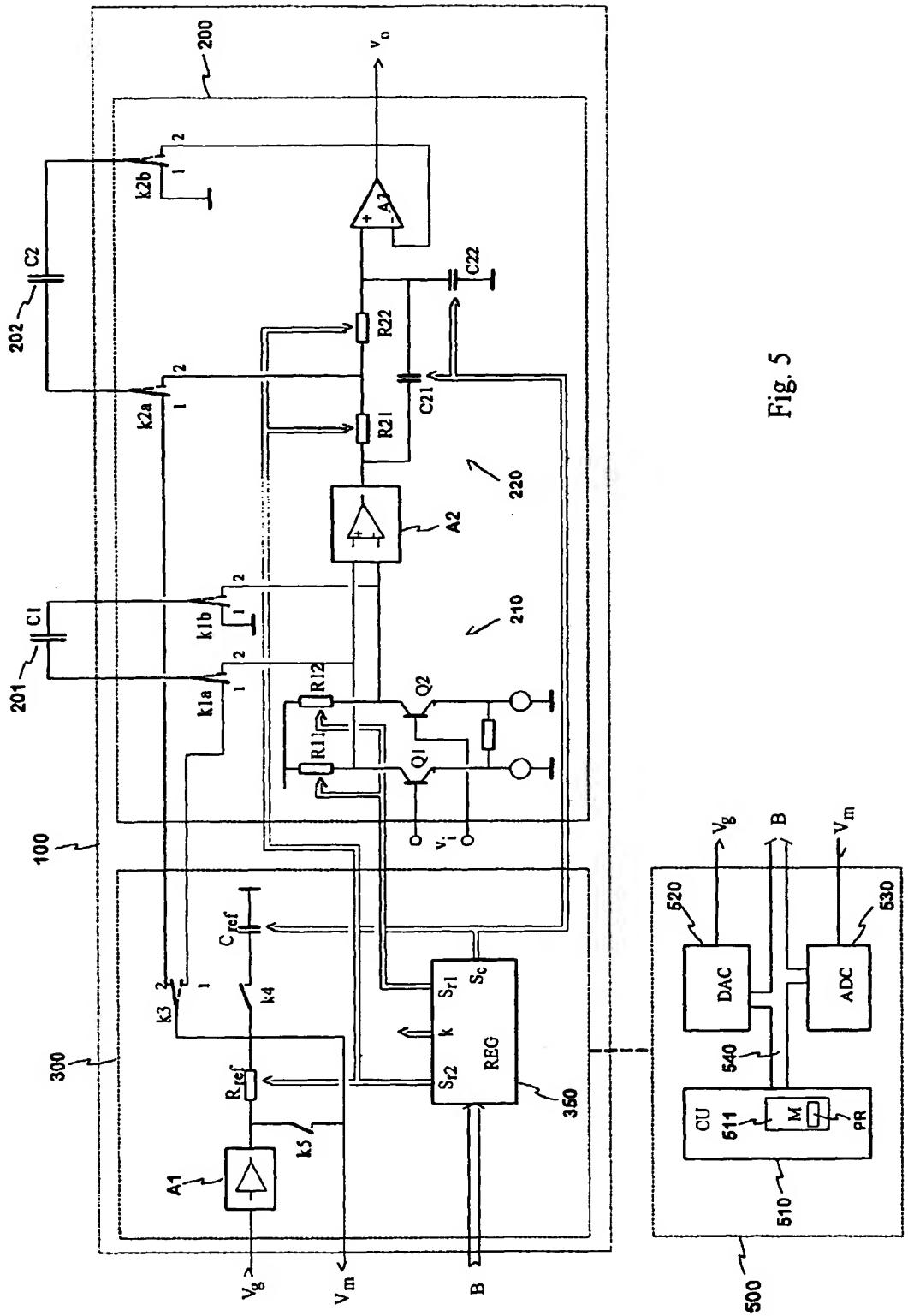

200
v_o
k2b
A3
C2
202
C22
R22
C21
R21
k2a
220
A2
C1
201
k1b
k1a
210
R12
R11
Q2
Q1
v_i
100
C_{ref}
k3
k4
300
R_{ref}
k5
A1
S_{r1}
S_c
k
REG
S_{r2}
350
V_g
V_m
B
V_g
B
V_m
520
530
DAC
ADC
540
CU
511
M
PR
510
500

Fig. 5

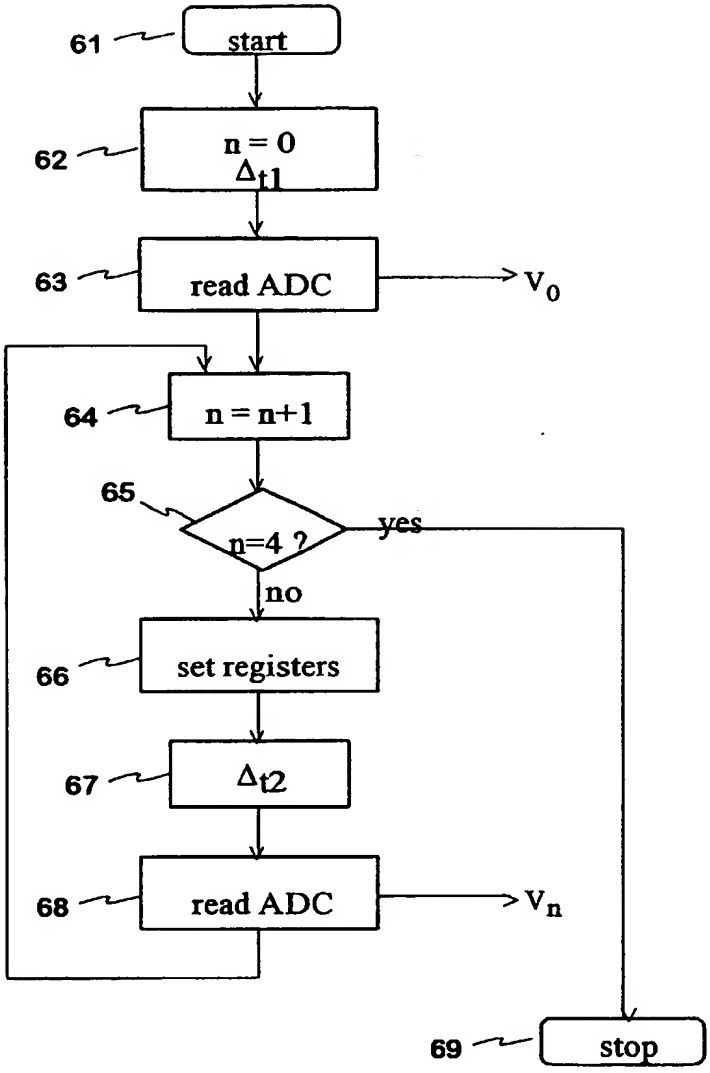

61
start
62
n = 0
Δt1
63
read ADC
V0
64
n = n+1
65
n=4 ?
yes
no
66
set registers
67
Δt2
68
read ADC
Vn
69
stop

Fig. 6

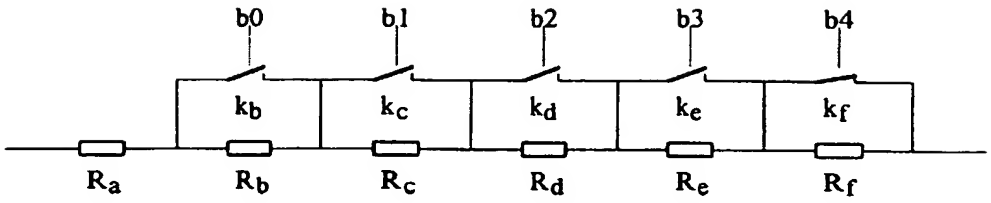
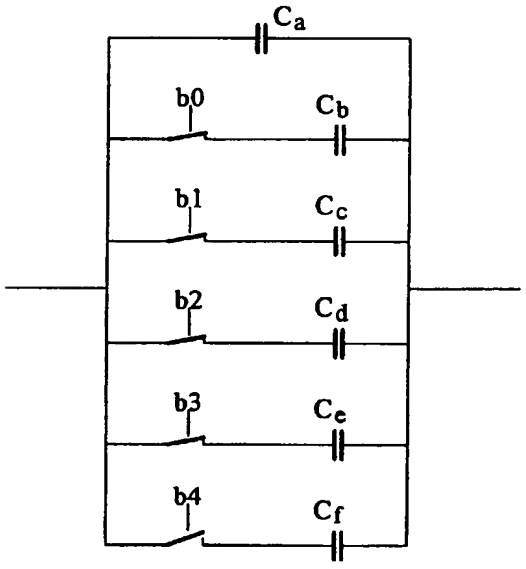


Fig. 7a

$S_r = b0\ b1\ b2\ b3\ b4$



$S_c = b0\ b1\ b2\ b3\ b4$

Fig. 7b